Intellectual Property Office

BL O/1218/24

24 December 2024

PATENTS ACT 1977

APPLICANT	Cantor Technologies Ltd
ISSUE	Whether application GB2210160.4 complies with Section 1(1)(b) of the Patents Act 1977.
HEARING OFFICER	Laura Starrs

DECISION

Introduction

1 WO 2021/140310 was filed on 11 December 2020, claiming a priority date of 10 January 2020. The application entered the national phase as GB2210160.4 on 11 July 2022, and was published as GB 2606109 A on 26 October 2022. The normal, un-extended period for putting the application in order ended on 10 September 2024. The applicant has been granted an extension to that period which is currently due to end on 10 January 2025.

2 Despite several rounds of correspondence, the applicant was not able to persuade the examiner that claims 1 – 8 in the application provided an inventive step, as required by Section 1(1)(b) of the Patents Act 1977 (hereinafter the Act). Therefore, the applicant requested a decision by a Hearing Officer, based on the papers on file. The matter has accordingly come before me.

3 The latest claims on file are those submitted in the main request on 10 September 2024. Alongside that set of claims an auxiliary set of claims were also submitted. The auxiliary request only comprised method claims which are similar in scope but not identical to claims 9 – 13 of the main request claims. In the pre-hearing report of 23 September 2024, the examiner objected to claims 1-8 of the main request claims as being obvious. This is the issue on which I have been asked to decide upon.

4 I note that the examiner has not objected to method claims 9 to 13 of the main request which they considered to comprise the subject matter of the auxiliary request claims. I have not been asked to decide on the allowability of the method claims and my decision is limited to the issue of obviousness of claims 1 – 8 of the main claims.

The Application

5 The application relates to the formation of a through hole vertical interconnect access (via) in printed circuit boards (PCBs) to improve vertical transmission of high frequency signals between layers of the PCB. The application discloses a

substantially planar multiple layer substrate with a via formed by drilling, at an angle, three times through at least one layer of the substrate where the inner surface of the via is provided with at least two conductive tracks for the transmission of high frequency electromagnetic signals.

Claims

6 Claim 1 as filed in the main request on 10 September 2024 is as follows (letters in parentheses added for reference purposes):

1. A substrate comprising

(a) at least two layers, wherein each layer comprises an insulation portion having a conductive portion on either side, wherein the substrate is substantially planar and is delimited by a substantially planar first face and a substantially planar second face that is substantially parallel to the first face of the substrate,

(b) the substrate further comprising a vertical interconnect access or 'via' extending through at least one layer of the substrate for the transmission of high frequency electromagnetic signals via conductive tracks extending through at least one layer of the substrate,

(c) the via comprising: a primary hole and two secondary holes drilled through at least one layer of the substrate,

(d) wherein the primary hole is defined by a drilled inner surface and has an associated axis and a diameter D1 corresponding to a diameter of a drill bit used to form the primary hole, and

(e) wherein each secondary hole has an associated axis and a diameter D2 corresponding to a diameter of a drill bit used to form each secondary hole,

(f) wherein the axes of the secondary holes are separated by a separation distance, S,

(g) wherein the primary and secondary holes are located at an angle which deviates from the orthogonal by up to +/- 15 degrees to the substantially planar first and second faces so that the length of each hole is greater than the thickness of the substrate layer(s) through which the via extends, and

(h) wherein the inner surface of the primary hole is provided with an electrically conductive coating and

(i) wherein each secondary hole overlaps the primary hole at a respective overlap region, such that the inner surface of the primary hole is interrupted at the respective overlap regions so that the electrically conductive coating is not present at the overlap regions such that the inner surface is provided with at least two separate conductive tracks and the via is divided to form two separate signal paths for transmission of signals from one layer of the substrate to another layer of the substrate; and

(j) wherein each conductive track is electrically isolated from the other conductive track(s) at the overlap regions and

(k) wherein the dimensions of the separation distance, S, the diameters D1, D2 of the primary and secondary holes, and the length of the via through the substrate are selected to determine the characteristics of the via and enable impedance matching.

7 I note that, as required by feature (b), the via, and the conductive tracks passing through it, must be suitable for carrying high frequency signals, but the via is not limited to only transmission of high frequency signals.

8 The primary and secondary holes are defined, in feature (g), as having a length greater than the thickness of the substrate. Therefore, the angle by which they deviate from the orthogonal must be non-trivially different from 0 degrees, but other than this there is no set minimum deviation.

9 I note that, as feature (i) provides for overlap between each of the secondary holes and the primary hole, then there will be only a single void formed in the substrate, by the three drilling operations.

The Law

10 Section 1(1) of the Act states:

> *1(1) A patent may be granted only for an invention in respect of which the following conditions are satisfied, that is to say –*
>
> *(a) the invention is new;*
>
> *(b) it involves an inventive step;*
>
> *…*

11 Sections 2(1) & 2(2) of the Act read:

> *2(1) An invention shall be taken to be new if it does not form part of the state of the art.*
>
> *2(2) The state of the art in the case of an invention shall be taken to comprise all matter (whether a product, a process, information about either, or anything else) which has at any time before the priority date of that invention been made available to the public (whether in the United Kingdom or elsewhere) by written or oral description, by use or in any other way.*

12 Section 3 of the Act states:

> *3 An invention shall be taken to involve an inventive step if it is not obvious to a person skilled in the art, having regard to any matter which forms part of the state of the art by virtue only of section 2(2) above (and disregarding section 2(3) above).*

13 In addition to statute, in *Windsurfing*[1] the Court of Appeal held that the question of obviousness

> "has to be answered, not by looking with the benefit of hindsight at what is known now and what was known at the priority date and asking whether the former flows naturally and obviously from the latter, but by hypothesizing what would have been obvious at the priority date to a person skilled in the art to which the patent in suit relates."

14 The four step test used in *Windsurfing* was reformulated by the Court of Appeal in Pozzoli[2] as follows:

> *(1) (a) Identify the notional "person skilled in the art"*
> *(b) Identify the relevant common general knowledge of that person;*
> *(2) Identify the inventive concept of the claim in question or if that cannot readily be done, construe it;*
> *(3) Identify what, if any, differences exist between the matter cited as forming part of the "state of the art" and the inventive concept of the claim or the claim as construed;*
> *(4) Viewed without any knowledge of the alleged invention as claimed, do those differences constitute steps which would have been obvious*

Analysis

Step 1: Identify the notional person skilled in the art and identify the relevant common general knowledge of that person

15 In their letter of 15 March 2023, the applicant considered the person skilled in the art to be an electronics engineer. In their view, such a skilled person would be aware of all methods and features used and known in the design of circuits including methods of making a through hole via in a PCB with more than one conductive track. The applicant has also included an awareness of single angled vias used in PCBs in their identification of the common general knowledge. The applicant further acknowledged that such a skilled person would be aware that conductive tracks in vias can carry electromagnetic (EM) signals and that carrying high frequency radio signals through such tracks has high losses. Further, the applicant acknowledged that the skilled person would be aware of the importance of controlling impedances on a PCB.

16 In the examination report of 5 April 2024, the examiner identified the person skilled in the art as a multiple-layer printed circuit board designer/engineer who has regard for the electrical design of PCBs and to methods of manufacturing them. The examiner maintained this definition of the skilled person in the subsequent examination report of 1 May 2024 and in the pre-hearing report of 23 September 2024.

17 The applicant has not contested the examiner's definition of the person skilled in the art in any of their correspondence. It is also notable that the application as filed is directed towards to the formation of through hole vias in PCBs to improve vertical transmission of high frequency signals. Therefore, I think the extra specificity in the

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[1] *Windsurfing International Inc. v Tabur Marine (Great Britain) Ltd* [1985] RPC 59
[2] *Pozzoli SPA v BDMO SA* [2007] EWCA Civ 588

examiner's identification is helpful and I identify the person skilled in the art as an electronics engineer involved in the design and manufacture of multiple layer printed circuit boards.

18 The examiner disagreed with the applicant's general statement that the common general knowledge would include all methods and features used and known in the design of circuits. However, they did agree, in the exam report of 5 April 2024, that the common general knowledge would include aspects of transmission line design and their characteristic impedances.

19 In the examiner's view, it is common general knowledge that impedance matching of high frequency signal transmission lines with an interconnecting via will always be a design constraint. Consequently, the skilled person will pay attention to the shape and layout of the planar conductive tracks and the shape and layout of via conductors and the surrounding environment such as the substrate and filler materials and any grounding conductors near the signal conductors. I agree with this view.

20 I also consider that, in the absence of any specific teaching in the description and in order to satisfy the sufficiency requirements, the common general knowledge also includes how variation in the length, size and relative location of the conductive tracks affects the impedance.

21 I also consider that the skilled person would know that factors other than the location, size and shape of the conductors affect the impedance. This includes factors such as the materials used in the substrate, the conductive tracks and any non-conductive material filling the via.

Step 2: Identify the inventive concept of the claim in question or if that cannot readily be done, construe it

22 In the pre-hearing report, the examiner identifies the inventive concept as:

> A via for connecting planar signal conductors at different levels of a planar multi-layer substrate, where the via comprises a primary hole, formed by mechanical drilling, though the substrate having a conductive inner surface that is interrupted at two spaced locations by two secondary holes which have removed material from that surface, these holes also formed by mechanical drilling, such that the via provides two electrically isolated conductive paths, where the three holes are formed by drilling at an angle away from orthogonal of up to 15 degrees such that the holes are longer than the thickness of the substrate.

23 In reaching this view of the inventive concept, the examiner has construed claim 1 as the resulting apparatus characterised by features formed by the constructional method steps used to form the features. They did not consider the claim to be limited by reference to selecting the diameters and separation of the holes used to form the via. Neither did they consider the claim to be limited only to the constructional method steps, but to the features that are present in the final apparatus as a consequence of the method steps. I agree with the examiner's view that the

substrate of claim 1 is not limited by the constructional method steps used to form the features of the claimed substrate.

24 The applicant has not in any of their correspondence dated 12 August 2024, 10 September 2024 or 10 October 2024 provided any explicit statements of their view of the inventive concept. However, they have consistently highlighted the importance to the invention of selecting the four variables (the separation distance, S, the diameters D1, D2 of the primary and secondary holes, and the length of the via) to enable impedance matching. This aspect is missing from the examiner's formulation of the inventive concept.

25 The applicant has also highlighted the significance of the conductive tracks carrying high frequency electromagnetic signals, and this is another aspect missing from the examiner's formulation of the inventive concept, see correspondence dated 10 October 2024. This isn't to say that the via is only for high frequency signals, just that it must be suitable for such signals, amongst others.

26 Accordingly, I have adopted a modified formulation of the examiner's inventive concept which is as follows:

> A substantially planar multiple layer substrate with a through hole via having an inner surface with at least two conductive tracks for the transmission of high frequency electromagnetic signals whereby the via is formed by drilling a primary hole with diameter D1 and two secondary holes each with diameter D2 and each secondary hole overlaps the primary hole such that the inner surface of the primary hole is interrupted and doesn't contain electrically conductive material in the overlap regions and the primary and secondary holes have a length greater than the thickness of the substrate layers the via extends through and the holes deviate from the orthogonal to the plane of the substrate by up to 15 degrees, and diameters D1, D2, length of the via and the distance between the secondary holes are selected to determine the characteristics of the via and enable impedance matching.

Step 3: Identify what, if any, differences exist between the matter cited as forming part of the "state of the art" and the inventive concept of the claim or the claim as construed

27 The examiner has cited 6 documents:

D1 WO2007/086961 A2 (VIASYSTEMS)

D2 US2007/0033457 A1 (PARK)

D3 US2012/0048610 A1 (HSU)

D4 KR20180075171 A (LG)

D5 US2018/070443 A1 (LEITGEB)

D6 JPS63-124595 A (HITACHI)

28 All of these documents were published before the declared priority date (10 January 2020), such that they are part of the state of the art under Section 2(2) of the Act. The examiner has identified these documents as forming two sets:

- Set A (D1 and D2) demonstrating a via having multiple isolated conductors formed by a method of drilling overlapping hole; and
- Set B (D3 – D6) each demonstrating forming a via with a hole at an angle away from perpendicular relative to a substrate surface.

Document D1

29 D1 discloses a method (see figures 2A-2G) of forming a through hole via, then coating the substrate and inner surface of the hole with copper. The hole is then filled, and the surface patterned and then holes 24 and 26 are formed leaving two isolated conductive tracks in the through hole via. D1 also discloses in paragraph 24 that the sizes of the holes 24 and 26 can be varied.

30 D1 differs from the inventive concept in that it doesn't disclose that the through hole via could be anything other than orthogonal to the substrate surface. While the description doesn't explicitly call for an orthogonal via, that is the implicit disclosure from the drawings which only show vertical vias. D1 also does not teach selecting the relative location or length of the via for any purpose nor does it teach adjusting the size of the secondary holes for controlling impedance. Finally, D1 differs from the inventive concept in that it does not disclose that the conductive tracks are suitable for high frequency signals.

Document D2

31 D2 discloses (in figures 3 and 4) a multilayered circuit board which has a via hole (131) the inner surface of which has two conductive tracks (137a and 132a). The via hole is formed from a cylindrical primary hole (131a) and two cylindrical secondary holes (131b and 131c) which overlap the primary hole such that the inner surface of the primary hole is interrupted and doesn't contain electrically conductive material and the two conductive tracks allow for signals to be transmitted from the top tracks (125,120) to the bottom tracks (140 and 145). Paragraph 38 discuss the importance of matching the impedance of the conductive tracks in the via hole to the impedance of the tracks of the surface of the substrate. D2 further discloses that to achieve this impedance matching consideration is given to the size and placement of the primary and second holes (and also the shape of the holes) and notes that the length of the via hole will affect the impedances. D2 explicitly teaches varying the separation distance and diameters of the primary and secondary holes, and implicitly teaches that the length of the via through the substrate can be varied for impedance matching.

32 D2 differs from the inventive concept in that it doesn't disclose that the angle of the via hole could be anything other than orthogonal to the substrate surface. While the description doesn't explicitly call for an orthogonal via, that is the implicit disclosure from the drawings which only show vertical vias. D2 also does not explicitly teach that the conductive tracks are suitable for transmission of high frequency signals.

Document D3

33 D3 discloses a printed circuit board with a single via designed at a slantwise angle to the PCB to reduce the signal transmission distance of the via and thus the signal transmission loss. This reduction in distance is achieved for paths going through and across the via (considering figure 1 the path goes between 12 and 32).

34 D3 does not disclose multiple tracks in the via, and hence there are no secondary holes. It also does not disclose that the angle is less than 15 degrees or that the conductive tracks are suitable for high frequency signals.

Document D4

35 D4 discloses a multiple layer PCB substrate with a diagonal via hole formed by drilling. As with D3 the reason for a diagonal hole is given, in paragraph 42, as shortening the via.

36 D4 differs from the inventive concept in that it doesn't disclose multiple tracks in the via, secondary holes, that the maximum angle of the hole is 15 degrees from the vertical, or that the track is suitable for high frequency signals.

Document D5

37 D5 discloses a multilayer PCB which has through crossing connections formed non-orthogonally to a planar surface of the PCB. The reason for angling the connections is to counteract warping tendencies of the PCB. The angle is preferably between 2 and 10 degrees from the orthogonal - greater inclination uses too much material and lesser inclination doesn't reduce warping sufficiently (see paragraph 14). The connection through the PCB may be used for high frequency signals (see paragraph 81).

38 D5 differs from the inventive concept in that it doesn't disclose multiple conductive tracks in the via, and hence no secondary holes. It also doesn't discuss any effect on impedance.

Document D6

39 D6 discloses a substrate with an oblique through hole. The reasoning behind using an oblique through hole is around providing greater selection in the layout on the surface.

40 D6 differs from the inventive concept in that it doesn't disclose multiple conductive tracks in the through hole and consequently, no secondary holes, nor does it discuss the appropriate angles for the through hole to be formed, the use of high frequency signals or any effects on impedance.

<u>Step 4: Viewed without any knowledge of the alleged invention as claimed, determine whether those differences constitute steps which would have been obvious to the person skilled in the art</u>

41 The examiner has argued that the differences from the inventive concept of either of D1 or D2 are demonstrated in each of document D3, D4, D5 and D6, such that the

combination renders claims 1-8 obvious. In the examiner's view it would be obvious for the skilled person to take the teaching of either D1 or D2 and modify it such that the via is formed at an angle by providing angled drill holes. In reaching this conclusion the examiner considered that an angled via was part of the common general knowledge. The examiner noted that only one of the documents (D5) provides a range of possible angles. However, they considered the person skilled in the art would find it obvious to try the 15 degree range as set out in claim 1 of the main request

42 The examiner has also put forward an alternative argument that either D1 or D2 might be considered with one of D3, D4, D5, or D6. The examiner noted that the reasons for producing an angled via in D3, D4, D5, or D6 are different to matching the impedance of the signal lines. In D3 and D4 the purpose of using an angled via is to reduce the signal transmission distance. In D5 the reason for angling the vias is to counteract warping of the PCB and in D6 the reason for angling the vias is to provide greater selection in in the layout of connection on the surfaces of the PCB.

43 The examiner appears to have argued that in using an angled via for the reasons set out in D3, D4, D5, or D6 and combining that with the teachings of either D1 or D2, the skilled person would arrive at the inventive concept without any prior knowledge of the alleged invention.

44 The applicant disagrees for various reasons, which are set out in the letters of 10 September and 10 October 2024. The applicant points to the fact that D3 – D6 only disclose single vias formed at an angle. None of the cited prior art mention creating several overlapping angled vias. The applicant argues that there are significant impediments to forming separate conduction paths within angled vias, for example due to the difficulty in aligning such closely spaced inclined holes within a substrate. In the applicant's view, this would be a factor that would dissuade a skilled person from combining the teachings of D1 or D2 with that of D3 – D6.

45 Secondly, the applicant argues that none of the prior at documents mention impedance matching nor teach any of the four associated variables of the present claim 1 (the separation distance, S, the diameters D1, D2 of the primary and secondary holes, and the length of the via).

46 Thirdly, the applicant points to the surprising and dramatic improvement in performance, especially at high frequencies, of the alleged invention. They also have stated that there is no motivation to combine the teachings of the prior art documents at low frequencies and that the documents disclosing angled vias do not relate to high frequency substrates which enables impedance matching.

47 Finally, the applicant also points to the age of the document stating that if it were obvious to combine the prior art to achieve the outcome of claim 1, such a product would have been created much sooner. The justification of this argument is that the move to high frequencies driven by the needs of different sectors, e.g. wireless communications and automotive radar, has not previously led to the creating of the claimed invention.

48 Having considered all the prior art cited, I am of the view that D2 is the closest to the inventive concept. D2 is silent on the issue of carrying high frequency signals.

However, I note that claim 1 of the main request merely requires the vias to be suitable for high frequency signals and it is therefore not a limiting feature of the claim. As noted above the person skilled in the art will be aware that conductive tracks in through hole vias can carry electromagnetic (EM) signals and that carrying high frequency radio signals through such tracks has high losses. Therefore, while D2 is silent on whether it is suitable for carrying high frequency signals I consider that the person skilled in the art would consider applying the teachings of D2 to high frequency signals.

49 The applicant has argued that none of the prior art mentions impedance matching. However, D2 discusses, at paragraph 38, the importance of matching the impedance of the conductive tracks in the via hole to the impedance of the tracks of the surface of the substrate. D2 further discloses that to achieve this impedance matching consideration is given to the size and placement of the primary and second holes (and also the shape of the holes) and notes that the length of the via hole will affect the impedances.

50 The applicant has also argued (in the letters dated 1 November 2022 and 15 March 2023) that the vias of D2 would be unsuitable for carrying different signals. However, I note paragraph 51 of D2 which describes a pair of vias that are formed on the inner wall of a via-hole where the first via carries a reference signal for the signal that is transmitted to the second via.

51 Therefore, D2 differs from the inventive concept only in that it does not disclose vias formed at an angle of up to 15 degrees from the orthogonal.

52 I consider that this difference would be obvious to the person skilled in the art based on the teachings of D2 and their common general knowledge. I agree with the applicant that angling via holes, *per se*, is part of the common general knowledge. Having an angle limited to 15 degrees from the orthogonal is not part of the common general knowledge. However, the application as filed identifies no technical effect of such a selection of this range. Therefore, in accordance with *Dr Reddy's Laboratories (UK) Ltd v Eli Lilly & Co Ltd* [3] I consider the selected angle to be merely an arbitrary selection which doesn't confer an inventive step.

53 D2 teaches the skilled person how to match the impedance of conductive tracks by considering the length of the via hole as well as the size and placement of primary and secondary holes. The skilled person would know that angled through hole vias exist and that using an angled via changes the length of the via. Once the skilled person has decided to make the workshop modification of the set-up in D2 to use an angled via hole of less than 15 degrees, D2 teaches them how to select the other variables of the size and relative locations of the holes to achieve the desired impedance. Thus, I find that the combination of D2 and the common general knowledge as identified by the applicant renders claim 1 obvious.

54 Alternatively, I also consider that the difference with the inventive concept would be obvious to the person skilled in the art based on the teachings of D2 in combination with the disclosures of D3 – D6.

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[3] *Dr Reddy's Laboratories (UK) Ltd v Eli Lilly & Co Ltd* [2010] RPC 9

55 Documents D3-D6 provide various motivations as to why a skilled person would consider using an angled via hole. Using the figure 3 example from D2, then angling the holes with a slope from track120 towards track 140 means that, although the hole is longer (and so tracks 132a and 137a are longer) than the orthogonal, the reduction in tracks 120, 125, 140 and 145 achieve a reduced overall length of track for the signal in the same way as envisaged in each of D3 and D4.

56 If the set-up in D2 meant that the PCB was suffering from warpage then D5 teaches using an angled via hole to address that problem. Similarly, if the designer of a PCB starting with the disclosure of D2, found that they needed greater flexibility in how to arrange the circuitry then the disclosure of D6 teaches that angling the vias is a solution to this problem.

57 Once, the skilled person implementing a PCB with a multitrack via decides, to use an angled via, either because they are part of their common general knowledge, to reduce overall track length, prevent warpage or increase the layout flexibilities. Then D2 teaches them the importance of the length of the via in controlling the impedance, alongside knowing from D2 the importance of selecting the sizes, and relative locations of the holes for controlling the impedance.

58 The applicant suggests, in the letters dated 12 August 2024 and 10 September 2024, that the skilled person would be biased against having an angled via, because of various manufacturing difficulties. I consider that such difficulties are plausible and may result in such a bias. However, the description and claims do not provide any solutions to such difficulties, and I consider that this bias is only such that the skilled person would not angle the via absent a specific reason for doing. Various reasons for angling a via have been disclosed in the prior art (D3 – D6) as discussed above. Thus, the skilled person would know that angled vias are possible and carry benefits and consequently they would be motivated to try using an angled via.

59 I have also considered the question of whether having the via formed of multiple overlapping angled holes introduces any particular challenges as compared to having single angular holes. As the description presents nothing in terms of a solution to any technical challenge in manufacturing such holes, then the disadvantage of having manufacturing complexity is something the applicant has chosen to tolerate for the benefits of a multiple signal angled via. Therefore, I consider that the challenges of forming multiple overlapping angled holes is not sufficient to provide an inventive step.

60 The applicant has also submitted, in the letter dated 10 October 2024, that the prior art documents were filed many years ago and that because the invention is novel, then this is indicative that combining the teachings of the prior art documents is not obvious.

61 The skilled person might not have expected the design of the present application to be so effective at high frequency, but as Whitford J observed, in *Union Carbide Corporation (Hostettler's) Application*[4], "if in fact the step taken was an obvious step, it remains an obvious step however astonishing the result of taking it may be". I consider that this describes the current situation in that angling the via in D2 and

[4] *Union Carbide Corporation (Hostettler's) Application*, [1972] RPC 601

using it for high frequency signals are obvious steps to take, such that it is immaterial that it has a dramatic improvement in performance that the skilled person would not expect.

Dependent Claims of the Main Request

62 I note that the applicant has made no submissions at any point during the prosecution of the present application regarding the characterising features of claims 2-8 of the main request. However, it appears that the subject matter of dependent claims 2 – 8 comprise subject matter that is conventional which do not confer an inventive step. The holes in the via in D2 are shown with a uniform cross section with the two signal paths being in parallel and as part of a printed circuit board made of a dielectric material with patterned tracks thereon, which may have multiple vias which could extend through the entire substrate (see figure 11). D2 is silent as to what occupies the via after construction, however, using a non-conductive material would be an obvious choice. Therefore, I consider claims 2-8 of the main claims to be obvious for the same reasons as claim 1 above.

Method Claims of the Main Request and the Auxiliary Claims

63 As noted above I have not considered method claims 9 – 13 of the main request, nor the claims of the auxiliary request. However, I note that the examiner has not raised any objection to the method claims of the main request which they consider to comprise the subject matter of the auxiliary request. I will remit the application to examiner to complete their examination of the method claims noting that the period for putting the application in order is due to expire on 10 January 2025.

Decision

64 I find that claims 1 to 8 of the main request lack inventive step as required by section 1(1)(b) of the Patents Act 1977. Noting that the examiner has not raised any objection to method claims 9 to 13 of the main request, I remit the application to the examiner to complete examination before the period for putting the application in order expires on 10 January 2025.

Appeal

65 Any appeal must be lodged within 28 days after the date of this decision.

LAURA STARRS

Patent Examination Group Head